REMARKS

Claim Rejections – 35 U.S.C. § 112

Claims 31-43 were rejected under 35 U.S.C. § 112, ¶ 2, as begin indefinite. The amendments to the claims should overcome the indefiniteness rejection.

Claim Rejections – 35 U.S.C. § 102

Claims 31-38, 41-44, 46, and 47 were rejected under 35 U.S.C. § 102(b) as being anticipated by Haji, Japanese patent document 11-067957. It is respectfully submitted that the Japanese patent document to Haji is not a § 102(b) reference. Pursuant to §102(b), a person is entitled to a patent unless – "the invention was... described in a printed publication in this or a foreign country... more than one year prior to the date of application for patent in the United States." 35 U.S.C. § 102(b). Thus, greater than 12 months must separate the publication date of a foreign publication and an applicant's U.S. filing date. The Japanese patent document was published on March 9, 1999. However, the present application claims priority to an earlier application that was filed on August 25, 1999. Clearly, less than 12 months separate the publication date for the Japanese document and the earliest filing date to which the above-referenced application claims priority. As such, the Japanese patent document to Haji is not believed to be prior art pursuant to § 102(b).

The Examiner relies on a United States patent to Haji as an English translation of the Japanese document. However, the US patent is not necessarily a verbatim translation of the Japanese patent document. For example, Haji's U.S. patent claims priority to two different Japanese applications, one being the above-referenced Japanese patent document. Also, the figures in the two documents are not in agreement. For example, the above-referenced Japanese patent document has Figures 1-10 whereas the U.S. patent has Figures 1-17. Thus, the U.S. patent to Haji is not merely a translation of the Japanese patent document. Nevertheless, in the interest of furthering prosecution of this application an attempt is made to respond to the rejection based on Haji's U.S. patent.

Haji fails to teach or suggest a first gold coating on solder ball bond pads that is 0.25 microns to about 0.3 microns thick, where the same first gold coating and a second gold coating form a composite gold coating on wire bond bond pads. (See claim 31.)

First, Haji fails to disclose a first gold coating on solder ball bond pads that is 0.25 microns to about 0.3 microns thick. Where the prior art teaches a value or a range that is very close to, but does not overlap or touch the claimed range, the claimed range is not anticipated. See M.P.E.P. § 2131.03 ¶ III. That is, to anticipate under §102 the reference must disclose exactly what is claimed; where there are differences between the referenced disclosure and the claim, the rejection must be based on § 103. *Id.* Referring to Figure 15 of the U.S. patent to Haji, the gold layer 62 on the surface of electrode 16 is about 0.01 to 0.2 microns thick, preferably 0.01 to 0.15 microns thick. Column 6, lines 9-12. However, pursuant to Haji, gold layers having a thickness above 0.2 microns interfere with the bonding force of solder bumps. Column 1, lines 26-59. Because Haji considers gold layers greater than 0.2 microns to be detrimental to bonding with solder bumps, it is respectfully submitted that Haji's upper limit for layer 62 is 0.2 microns, not more. In other words, Haji's range would not extend to 0.25 microns or above. Accordingly, Haji does not anticipate because he does not disclose exactly what is claimed.

Second, Haji fails to render claim 31 as obvious because the first gold coating is part of a composite gold coating on the wire bond bond pads. See claim 31. That is, pursuant to claim 31, the first gold coating coats solder ball bond pads and wire bond bond pads; a second gold coating coats only the wire bond bond pads. The second gold coating and first gold coating, which is 0.25 microns to about 0.3 microns thick, form a composite coating on the wire bond bond pads. Thus, the thickness of the first claimed gold coating contributes to the thickness of the composite gold coating on the wire bond bond pads. Haji fails to disclose a composite gold coating. See Office action, page 7. As such, a first gold coating of 0.25 to about 0.3 microns thick would not be obvious in view of Haji alone.

Third, Haji fails to render claim 31 obvious because 0.25 microns of gold provides a coating on solder ball bond pads that is sufficiently small to reduce solder ball joint embrittlement, yet thick enough to prevent oxidation. Specification, page 5, lines 17-25. The U.S. patent to Haji fails to disclose a gold coating having both properties. Thus, the thickness of the claimed first gold coating on the solder ball bond pads is important in that it contributes to the composite gold coating on the wire bond bond pads and prevents oxidation and solder ball joint embrittlement on the solder ball bond pads. As such, it is respectfully submitted that Haji neither anticipates nor renders amended claim 31 obvious.

Forth, there is no suggestion or motivation to modify Haji in view of Watanabe. In the Office action, Watanabe is relied upon as teaching a composite gold coating. The rationale to modify Haji in view of Watanabe is to decrease the defects in the top layer of a conduction pad as stated by Watanabe. However, Watanabe does not indicate what defects are decreased. Thus, decreasing nonspecific defects without more is insufficient to be a suggestion or motivation to modify Haji.

Fifth, Haji and Watanabe teach away from each other. For example, Haji begins with a thick gold coating and reduces the coating on less than all electrodes. Column 5, lines 1-19; column 6, lines 1-13. In contrast, Watanabe begins with a first gold layer and places gold leaf over the first gold film. See Abstract. Thus, it is not apparent why one would be motivated to use two gold layers when Haji's teachings are contrary to Watanabe. Moreover, Watanabe forms gold layers on connection pads for solder and wire bonding in the same way, fails to discuss gold film thickness, and does not contemplate a connection pad for different types of bonding on the same substrate. See Abstract. For at least these reasons, there is no apparent reason to modify Haji in view of Watanabe. Thus, *prima facie* obviousness over the combination of Haji and Watanabe has not been established with respect to claim 31.

In sum, Haji alone or in combination with Watanabe does not render claim 31 or claims dependent thereon unpatentable. Under a similar analysis, claim 37 and respective dependent claims are also believed to be patentable over Haji alone or in combination with Watanabe.

Claim 44 was rejected as being anticipated by Haji. Claim 44 is directed toward an intermediate structure for an integrated circuit device. The structure comprises a first bond pad comprising a gold coated metal, the gold coating having a thickness of between about 0.1 and 0.5 microns and a second bond pad which is masked, the second bond pad comprising a nickel coated metal. The apparent issue with respect to the rejection of claim 44 is whether the resin 19 of Haji is masked as is understood by one of ordinary skill in the art. The resin 19 of Haji is used to seal the semiconductor element 12, electrode and gold wire 15. Column 3, lines 20-22. In contrast, the term masking is used interchangeably with the term patterning, and patterning includes creating features consisting of lines and spaces. See attached definitions from Semiconductor Technology, Griggs, Miller, Van Zant (eds.), pp. 65 and 77. Attached as Exhibit A. Haji fails to disclose that the resin 19 is used to create features consisting of lines and spaces. Accordingly, Haji does not anticipate claim 44 or claims dependent thereon.

In view of the amendments and remarks herein, the application is believed to be in condition for allowance. The Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees, including extension of time fees, or credit any overpayment to Deposit Account No. 20-1504(MCT.0046C1US).

Respectfully submitted,

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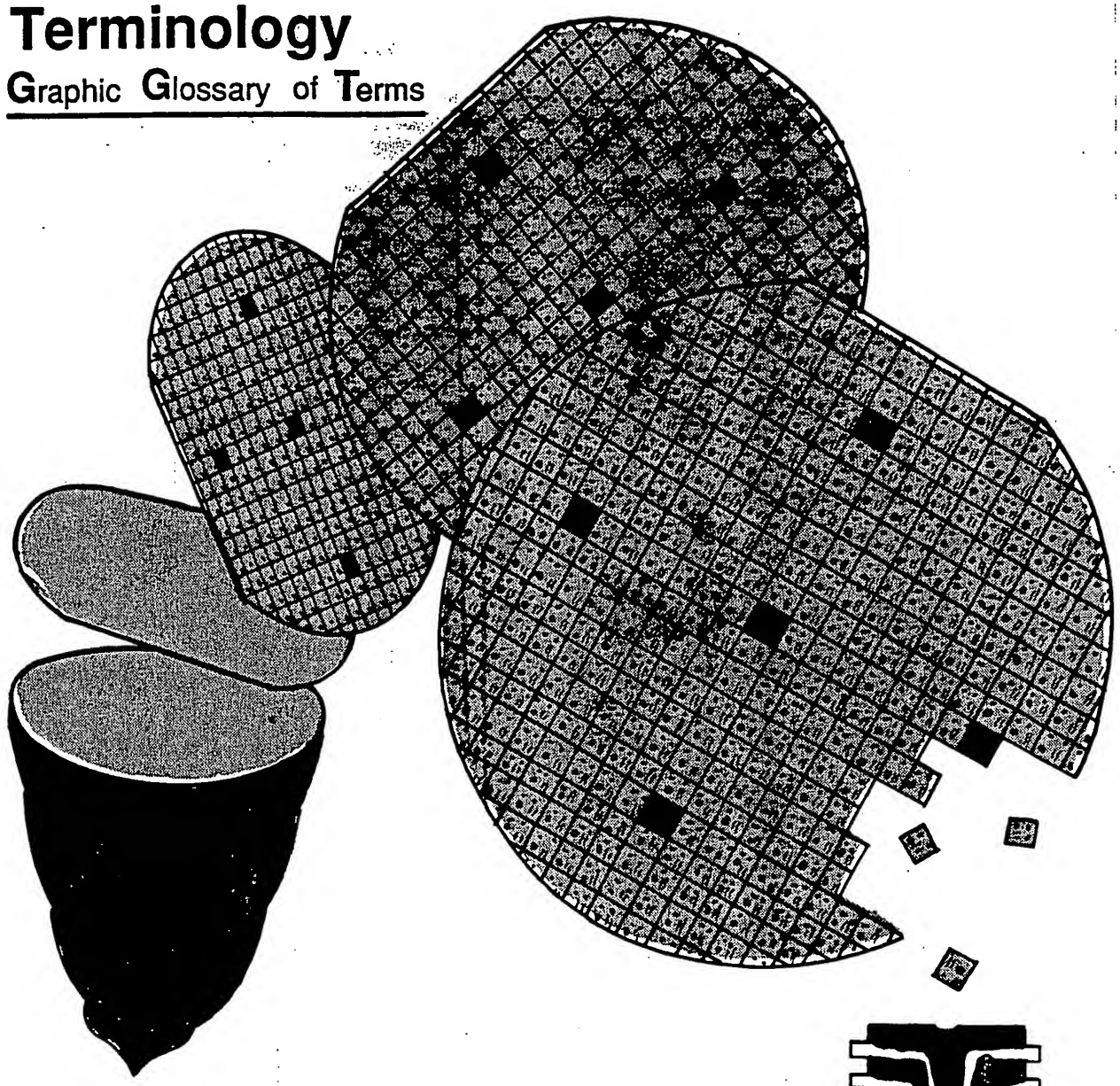
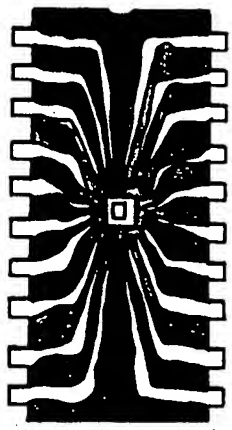
Attachments—Exhibit A

Semiconductor Terminology

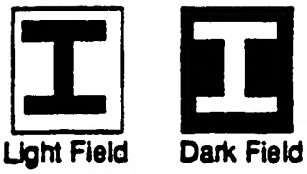
Graphic Glossary of Terms





B. Griggs
A. Miller
P. Van Zant

MASK POLARITY: a mask can be classified as either a "clear field mask" or a "dark field mask" and refers to patterns that are dominantly transparent or dominantly opaque.



Mask Polarity

MASKING: see "patterning"

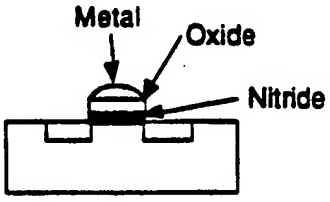
MEDIUM SCALE INTEGRATION (MSI): . Refers to chips with between 50 and 5,000 components each.

Integration Levels Chart

Level	Abreviation	# Components per Chip
Small Scale Integration	SSI	2 - 50
Medium Scale Integration	**MSI**	**50-5000**
Large Scale Integration	LSI	5000-100,000
Very Large Scale Integration	VLSI	100,000-1,000,000
Ultra Large Scale Integration	ULSI	over 1,000,000

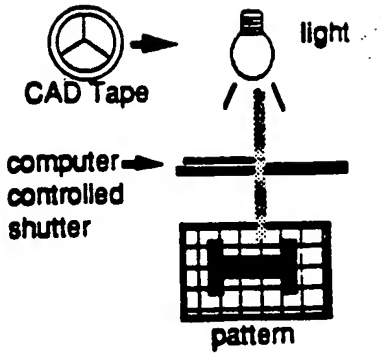
MEMORY: a circuit function which provides capacity for data or information storage.

MEMORY MOS (MMOS): A nonvolatile memory device structure that enables information to be retained during power shutdown.



MMOS Structure

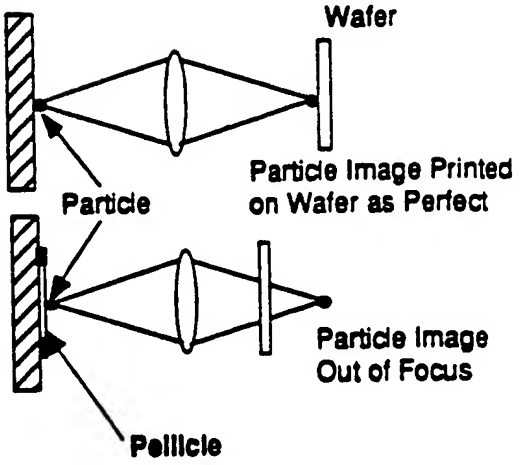
PATTERN GENERATOR: a machine comprised of a light source and computer controlled high speed shutter. A reticle blank coated with photoresist is placed on a stage and is moved under the shutter and light source systems to expose the reticle in the same pattern as the original digitized drawing.



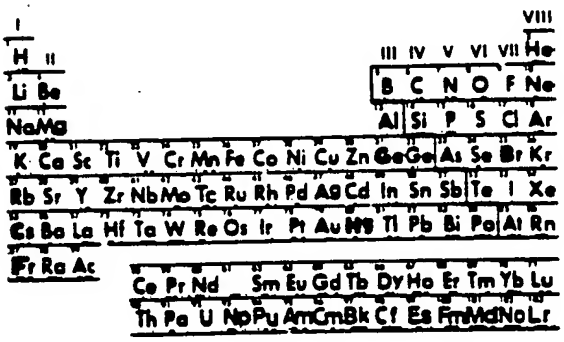
Pattern Generator

PATTERNING: method used to create features consisting of lines and spaces.

PELLICLE: a thin film of an optical grade polymer that is stretched on a frame and secured to a mask or reticle. This solves the problem of airborne dirt collecting on the mask and acting as an opaque spot. The image of the contamination is out of the focal plane during exposure and does not print on the wafer.



PERIODIC TABLE: the table of chemical elements arranged in rows and columns. Elements with similar properties are in the same column.



Periodic Table